Large-Signal Characterization of Dual-Gate Field Effect Transistors Using Load-Pull Measurements

Denis M. Drury, *Senior Member, IEEE,* David C. Zimmermann, *Member, IEEE,* and W. Alan Davis, *Member, IEEE*

***Abstract*—A new automated injected signal load-pull measurement system has been designed to operate from 8 to 12 GHz, with a range of injected signal power extending to 4 W. The system has been shown to be as accurate as the HP8510 network analyzer. The large signal intrinsic drain to source resistance of an 1800 μm dual gate FET was measured on the load-pull system, and subsequently a variable power amplifier was designed using the load-pull data. The amplifier output phase variation of the variable power amplifier was 10° when operating at 31.3 dBm.**

I. Introduction

SMALL-SIGNAL parameters are of limited use when designing an oscillator or a large-signal amplifier operated in a mode other than class A. For these nonlinear applications, it is necessary to characterize the performance of the device when terminated with a source or load impedance other than 50 Ω. This "load-pull" measurement yields data for plotting contours of constant power versus load impedance on the Smith Chart. Load-pull is a large-signal measurement technique used to determine the load impedance required to effect the maximum transfer of power by a large signal transistor. Several techniques [1]–[7] have been presented for performing load-pull experiments.

This paper describes an automated load-pull measurement system using advanced network analysis equipment that is employed to obtain a nonlinear model for a power GaAs MESFET. The load-pull measurement technique used in this system is an implementation of the basic concept by Takayama [4]. This approach has two advantages over those using a physical output tuner [1]: 1) transmission losses in the measurement system can be easily corrected by a calibration; and 2) the magnitude of the load reflection coefficients greater than 1 can be realized. The system simultaneously measures gain and phase of the transmission path through the device under test (DUT) and the load impedance presented to the device. Transmission path phase variation, which is a function of gate-2 voltage (V_{G2}), was measured as the load impedance was varied over an impedance range that includes the maximum power impedance. The experimental procedure is described in Section IV. Verification of the system accuracy is demonstrated by comparing small-signal "load-pull" characteristics on a GaAs FET to small-signal data measured by the standard network analysis technique. Finally, both small signal and load-pull measurements were made to determine the optimum load impedance of an 1800 μm dual-gate FET. This procedure is used in place of the technique described earlier [8].

Load-pull measurements are performed using a signal injection system [9]. The device compression point is determined and maintained as well as dc bias conditions. The characterization includes determining the maximum power load impedance (maximum power transferred to the drain load) and various load impedance contours of a dual-gate device. Also, transmission phase performance is determined at each impedance as a function of gate-2 voltage.

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D. M. Drury and D. C. Zimmermann are with Microwave Products and Technology Division, Defense Systems and Electronics Group, Texas Instruments, Dallas, TX 75266.

W. A. Davis is with the Department of Electrical Engineering, University of Texas, Arlington, TX 76019-0016.

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II. Load-Pull Measurement Technique

A simplified block diagram of the injection load-pull system is shown in Fig. 1. A range of load impedances is presented to the DUT at the frequency of the source by controlling the magnitude and phase of the signal injected into the output port of the DUT. The device output impedance is a function of the injected signal and the transfer function of the DUT. This technique permits very accurate measurements because impedances are established at a calibrated measurement plane.

Takayama [4] demonstrated that the load impedance Y_L equals the negative of the device output impedance Y_D during large-signal operation as long as dc bias conditions and RF input power delivered to the device are maintained (Appendix). Thus,

$$Y_L = -Y_D \tag{1}$$

and consequently,

$$\Gamma_L = \frac{1}{\Gamma_D}. \tag{2}$$

The load impedance is determined by the ratio of the forward and reverse voltage waves at the output terminal of the device, and is controlled by adjusting the amplitude and phase of the signal incident at the output port. The device reflection coefficient depends on the device transfer function, dc bias conditions, and the large signal RF power delivered to the device. The signals a_1 and b_1 are incident and reflected signals on port 1, respectively, and are expressed as

$$a_1 = |V_i| \exp j(\omega t + \phi) \tag{3}$$

$$b_1 = |V_i|\Gamma_{di} \exp j(\omega t + \phi) \tag{4}$$

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where $|V_i|$ is the signal magnitude, Γ_{di} is the device input reflection coefficient, and ϕ is the signal phase. Similar expressions are obtained for a_2 and b_2 in terms of the magnitude of the output voltage $|V_o|, \Gamma_{do}$ the device output reflection coefficient, and the output reflection phase Θ. The value a_2 is provided by the system, so the measured value b_2 gives Γ_{do} and thus the load impedance at the calibration reference plane. The load reflection coefficient Γ_L is then

$$\Gamma_L = \frac{a_2}{b_2} = \frac{1}{\Gamma_{do}}. \tag{5}$$

To ensure that power is delivered to the load, the condition $|a_2| < |b_2|$ must be maintained, otherwise an equivalent passive load is not realized.

Independent one-port calibrations are performed at the input and outut test ports. Higher order error correction, such as the full 12 term error correction, is avoided because of the nonlinear nature of the device transfer function.

The accuracy of the load-pull system is enhanced by using a difference power measurement technique. This is accomplished, as described by Poulin [1], by using dual-directional couplers to measure the difference between the incident and reflected power applied to both ports of the DUT. A modified version of this technique was used in our approach that implemented a two-step procedure. This uses the average of the power reflected from a short and an open circuit in place of the DUT and a known amount of power into a 50 Ω termination. This calibration can be performed at the same time as the vector calibration for the network analyzer. A lowpass filter used at the output of the DUT suppresses harmonic power from the power measurement and provides a known harmonic termination impedance. This filter presents a high reflection to the DUT harmonics that approximates Takayama's [4] theoretical assumption of short circuited harmonics at the device terminals.

III. Measurement Procedure

Small signal S-parameters were measured on an 1800 μm FET with data referenced to the APC-7 connector interface using the HP8510 analyzer at 9, 10, 11, and 12 GHz. Incident power on the device input was -5 dBm to ensure small-signal operation. The device was placed in the load-pull system to determine the maximum power condition while maintaining identical RF drive and dc bias conditions.

The data (Table I) indicate that the calibration technique provides excellent accuracy during the measurement mode. Calibration is verified by measuring standard mismatched terminations. This accuracy is compared to the response measured on an HP8510 network analyzer. The two measurements were found to be identical. A second verification step was done by checking the accuracy of the reference planes with signals applied from a single source but from opposite directions. The greatest source of error is the resolution in the power meter at the maximum power level. An example of this resolution limitation is demonstrated from the 9 GHz measurements. The load impedances $Z_L = 18.75 - j24.4\,\Omega$ and $Z_L = 17.93 - j24.8\,\Omega$ cause no fluctuation in the output power. This represents a variation of 6% in Re $\{Z_L\}$ and 2% in Im $\{Z_L\}$.

TABLE I
Comparison of Small Signal Measurements With Load -Pull System Verifies its Accuracy

Freq. GHz	HP8510		Load-Pull System	
	S_{22}	Z_{22} Ω	$\Gamma_L = S_{22}^*$	Z_L Ω
9.0	.579∠ 121.5°	17.1 + j25.4	.561∠-122.3°	17.9 - j24.8
10.0	.597∠-16.6°	151.7 - j80.4	.608∠12.1°	172.7 + j71.3
11.0	.657∠-138.3°	11.8 - j18.1	.664∠139.1°	11.4 + j17.7
12.0	.702∠90.3°	16.9 + j46.8	.670∠-88.1°	19.6 - j47.7

The RF drive level for each port corresponds to the signal range expected in an actual circuit application. This range is based on the device size and gain. System calibration RF levels are chosen to be the midpoint of this measurement range. This minimizes accuracy dependency on the linearity of the load-pull system frequency converters. After the RF levels are established, both the power meters and the vector measurement system are calibrated to define reference planes at ports 1 and 2. The DUT, cascaded with a coaxial tuner on the input port, is connected into the system. To establish actual operating conditions, the tuner is adjusted to provide high return loss. The tuner now remains fixed for all subsequent load-pull measurements and the load impedance is adjusted strictly by the system injecting RF power into the output of the DUT. Typically the input match is better than 14 dB return loss. The device is removed, leaving the tuner in place. Then port 1 is recalibrated to eliminate the effects of the tuner from the measurements. After reconnecting the device into the load-pull system and applying bias voltages, the drain load impedance is measured. The quiescent point must be maintained to satisfy (1). This is done by keeping constant both dc bias and RF power delivered to the device input, $\frac{1}{2}(|a_1|^2 - |b_1|^2)$. To determine the maximum power load impedance, both the magnitude and phase of a_2 are varied. While this is done, the maximized power delivered to the load is recorded as $\frac{1}{2}(|b_2|^2 - |a_2|^2)$.

Once Y_L is determined for maximum output power, the phase variation of S_{21} is measured. An S_{21} "through" response calibration is performed with an 1800 μm dual-gate FET operating at the maximum output power point. This establishes a reference phase that is dependent on the maximum output power drain load. The S_{21} phase variation is measured by varying V_{G2} while maintaining this load impedance. Effectively, the magnitude of b_2 is reduced by adjusting V_{G2} to a greater negative value. As a result, the magnitude and phase of a_2 is adjusted during this measurement to maintain

$$\Gamma_{L\max} - \frac{a_2}{b_2} = \text{constant}. \tag{6}$$

IV. Dual-Gate FET Phase Variation

Power amplifier designs using dual-gate FET's have an additional degree of complexity when the power management capability is utilized. Liechti [11] and Pengelly [10] have demonstrated that gain increases as the gate-2 impedance

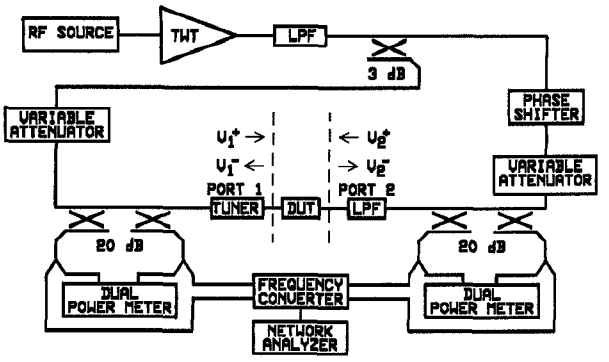

Fig. 1. Load-pull system simplified block diagram.

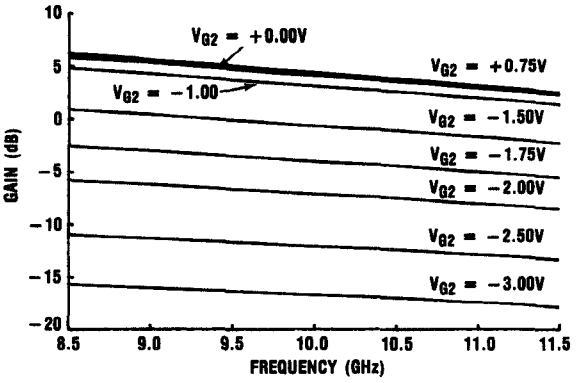

Fig. 2. Device $DG2$ small-signal gain as a function of gate-2 voltage.

is varied from a capacitance to an inductive termination for a fixed gate-2 voltage. The forward transmission phase variation of a dual-gate FET is 75° for a 20 dB gain variation. This phase variation was achieved at 10 GHz with a gate-2 reflection coefficient Γ_2 of $1\angle 153°$. The same characterization shows that S_{21} phase variation is 5° for the same gain variation with $\Gamma_2 = 1\angle -45°$. Previous results show that minimum phase variation is obtained as a function of V_{G2} for a short circuited gate-2 termination [8]. As a result, a compromise between power delivered to the load, phase performance, and efficiency is made in determining the proper gate-2 termination. Large-signal characterization of an 1800 μm dual gate FET is accomplished by load-pull measurements in the frequency range of 9–11 GHz. This characterization is focused on finding the optimum load impedance that yields maximum power delivered to the load while minimizing phase variation of the transmission path.

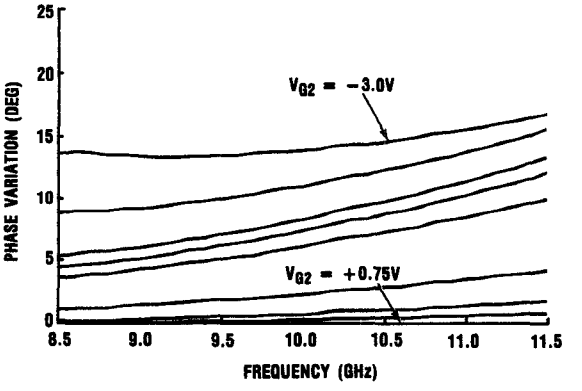

Fig. 3. Device $DG2$ small-signal phase variation as a function of gate-2 voltage.

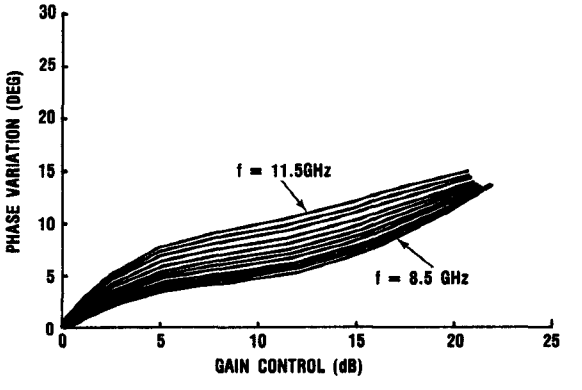

Fig. 4. Small-signal phase variation versus gain control is shown. The 0 dB gain control point is referenced to maximum gain for each frequency. Frequencies are 8.5–11.5 GHz, in 0.2 GHz increments.

V. Small-Signal Characterization

Initially, small signal S-parameters of the dual-gate FET's are measured on the automatic network analyzer where gate-2 is RF terminated as a short circuit by connecting it to on-device by-pass capacitors. Measurements are performed over a frequency range of 2–14 GHz and a gate-2 voltage of +0.75 to −3.00 V, while $V_D = 9$ V and $V_{G1} = -1.73$ V. The data in Fig. 2 show that approximately 22 dB of gain control is achieved for the device from 8.5 to 11.5 GHz. Gain control was minimal within a $VG2$ range of +0.75 to −1.00 volts. This information is used for two purposes. First, the accuracy of the small-signal model used in the design of the variable power amplifier is checked by device response. Second, this information is applied to device de-embedding so the drain bond wire inductance can be determined [13].

The small-signal S_{21} phase variation is shown in Fig. 3 for the same gate-2 voltage values and frequency range. The phase is referenced to $V_{G2} = +0.75$ V. As gate-2 voltage is increased to a larger negative value, phase variation increases to 15° at 10 GHz. This performance is expected for a slightly inductive gate-2 termination. Phase variation as a function of gain control is shown in Fig. 4. The 0 dB gain control point represents maximum gain.

VI. Large-Signal Characterization

Four basic characteristics require consideration for device characterization. They are: 1) power gain, 2) output power, 3) power control as function of gate-2 voltage, and 4) phase variation with respect to power control. Tucker [12] has shown that large signal device characterization using the load-pull method is superior to using large-signal S-parameters. While large-signal S-parameters are easier to implement, load-pull measurements are more useful in power amplifier design. Load-pull measurements are performed with drain terminations that are used in typical circuit applications. Associated

TABLE II
FREQUENCY CHARACTERISTICS OF DUAL GATE FET, $DG2$, AS MEASURED ON THE -0.7 dB CONTOUR

Freq. GHz	Power Out (dBm)	Power Added Efficiency (%)	Z_L (Ω)	Peak Phase Variation (deg.)
9.0	30.3	46.3	13.7 + j8.0	12.9°
10.0	30.0	42.9	12.7 + j7.8	19.8°
11.0	28.9	35.0	11.3 + j6.6	19.2°

circuit bias conditions and RF drive levels are determined and maintained during these measurements. Thus, load-pull measurements simulate actual circuit conditions.

Load-pull measurements were performed on two 1800 μm dual-gate FET devices. The first device, DG1, was measured at 10 GHz to determine the maximum power impedance and -1 dB and -2 dBm contours. The second device, DG2, was measured at 9, 10, and 11 GHz determining the maximum power load impedance at each frequency and the -0.7 dB power contour. All measurements were performed maintaining the identical dc bias conditions used during the small-signal characterizations.

The maximum power conditions required to obtain 2 dB gain compression were found by an iterative process. With V_{G2} set to +0.75 V, the compression level was measured for a given load impedance. If the 2 dB compression criterion is not met initially, then the input RF is adjusted. A new maximum power out, a new load impedance (simulated by RF injected into the device output port), and a new compression level are measured. Repeating this process establishes the required device compression condition. Once the maximum power out and load impedance are determined, V_{G2} is varied from +0.75 to -3.25 V in 0.25 V increments to measure the S_{21} phase variation.

The next characterization step is to measure the -1 and -2 dB load contours. With $V_{G2} = +0.75$ V, the load impedance is adjusted until power delivered to the load is reduced by 1 dB. This establishes the first impedance point on the -1 dB load contour. Holding this impedance constant, V_{G2} is again varied to measure S_{21} phase variation. This measurement procedure is continued until the -1 dB contour is determined. Device 1 load impedances for the maximum power delivered to the load and the -1 dB and -2 dB contours are shown in Fig. 5. The peak phase variation corresponding to 15 dB of power control is shown in Table II for the second device, $DG2$, for specific load impedances measured along the -0.7 dB contour. Peak S_{21} phase variation measures 7.9° for the same power control. Fig. 6 shows phase variation versus power control for $DG1$ when loaded at the maximum power impedance at $f = 10$ GHz. The second device, $DG2$, is similarly characterized at 9, 10, and 11 GHz.

The peak impedance shift for maximum power delivered to the load is less than $2.4 + j1.4\,\Omega$ from 9 to 11 GHz. The power delivered to the load associated with

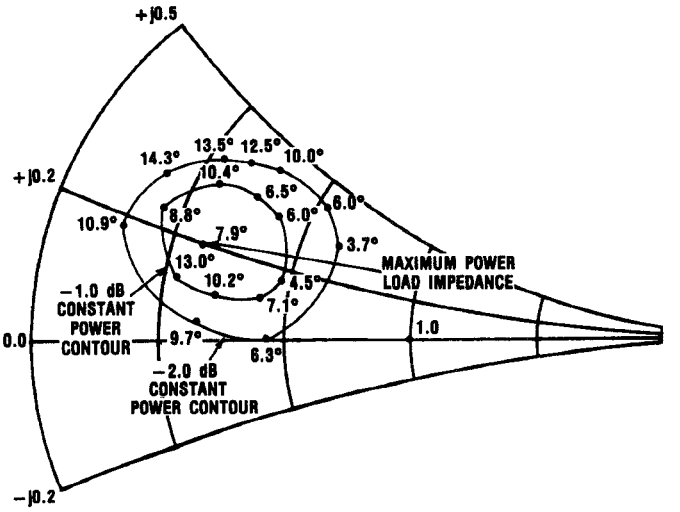

Fig. 5. Device $DG1$ maximum power impedance, -1 dB and -2 dB power contour impedances for $f = 10$ GHz. Maximum power and constant power contour impedances are defined for $V_{G2} = +0.75$ V. Also shown is phase variation at each impedance defined for 15 dB of power control.

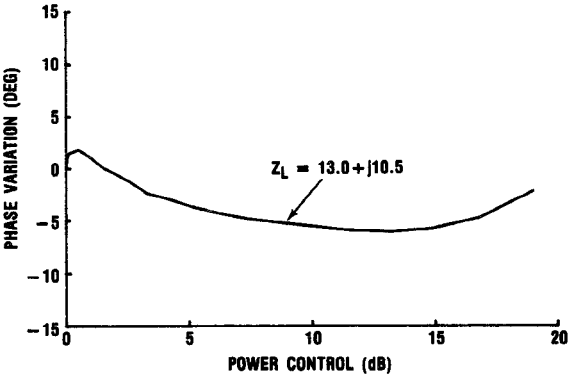

Fig. 6. Device $DG1$ phase variation versus power control for the maximum power load impedance at $f = 10$ GHz.

these impedances is within 0.3 dB, except at 11 GHz where it was 1.4 dB. The minimum phase variation occurs for a load impedance that is more inductive than the maximum output power impedance. In addition, a drain load exists that minimizes the transmission phase variation.

The last characterization step is removing the test fixture effect using the Through-Short-Delay [13] calibration technique. This technique establishes the measurement reference plane at the interconnecting microstrip network and device bond wire interface. The drain bond wire inductance was determined and removed by using the small-signal data for $V_{G2} = +0.75$ V. This 1-port datum is modeled as an inductance in series with a parallel RC network connected to ground. The parallel capacitance is the equivalent drain to source capacitance C_{DS}. The value of the bond wire inductance is adjusted in the circuit model to produce a constant C_{DS} versus frequency. The equivalent inductance values are 0.2 and 0.1 nH for devices $DG1$ and $DG2$, respectively. This corresponds to equivalent C_{DS} values of 0.57 and 0.58 pF for the two devices. The real part of

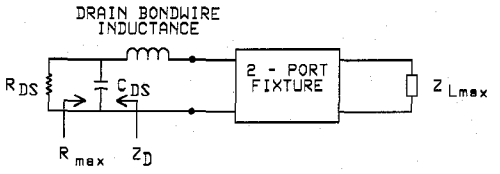

Fig. 7. One-port de-embedding network used to determine the drain to source resistance of the dual-gate FET.

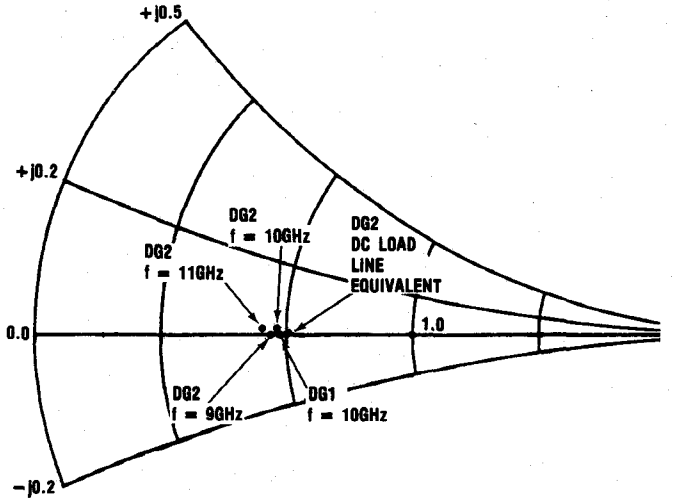

Fig. 8. Smith Chart plot of drain to source resistance required to achieve maximum power delivered to the load. Included is the loadline resistance.

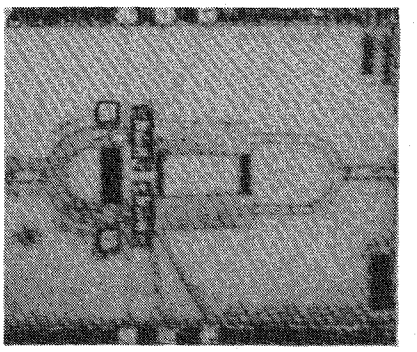

Fig. 9. Photograph of the variable power amplifier using two 1800 μm dual-gate FET's. The amplifier is oriented with the RF input port on the left and the RF output port on the right.

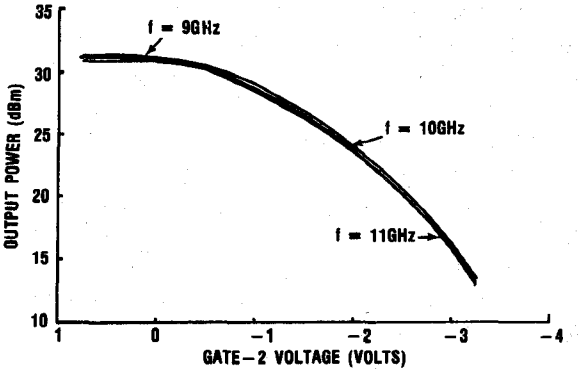

Fig. 10. Variable power amplifier output power versus gate-2 voltage.

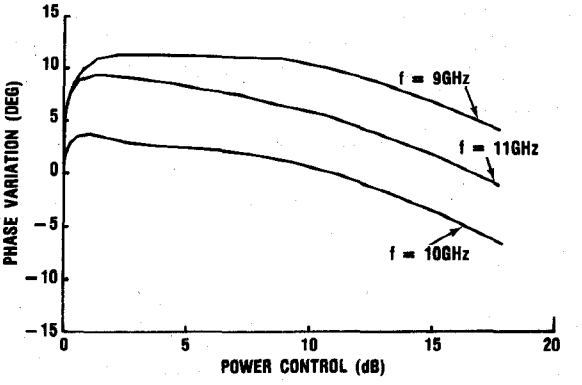

Fig. 11. Variable power amplifier S_{21} phase variation versus power control.

the maximum power load impedance is determined after the bond wire inductance and C_{DS} are known (Fig. 7). The load impedance that yields the maximum transfer of power is $Z_{L\max}$. The measured $Z_{L\max}$, together with the known value of bondwire inductance and C_{DS}, provides the value for R_{DS}.

The Smith chart plot in Fig. 8 of Re $\{Z_D\}$ for both devices shows the impedance points are tightly clustered at $Z = 24.0 + j0.0\,\Omega$. This is a significant result. It verifies the accuracy of the load-pull measurements and the technique used to remove fixture effects. As a final check, comparison of the load-pull response and the conventional load-line is performed. dc probe measurements show an equivalent load-line resistance of 25 Ω as plotted in Fig. 9.

VII. Variable Power Amplifier Design

A variable power amplifier was designed using the data provided by the load-pull characterization of two dual-gate FET's. The information obtained by the device characterization is used to optimize the load impedance for minimum S_{21} phase variation and for maximum output power. The optimum design load impedance is $14.6 + j10.4\,\Omega$. It is located inside the -0.7 dB constant power contour and near the region of minimum S_{21} phase variation. This design value is used because it provides adequate power delivered to the load while minimizing S_{21} phase variation. The drain load network is implemented using a two-stage Wilkinson power combiner. This design provides isolation between the drains of the two devices, thus maximizing amplifier stability. The amplifier shown in Fig. 9 produced 31.3 dBm of output power at 10 GHz. This amplifier has quiescent drain current that is identical to the characterized devices.

Amplifier gain under large-signal excitation was 31.3, 31.2, and 30.9 dBm at 9, 10, and 11 GHz, respectively. Power delivered to the amplifier for all frequencies was 21.1 dBm. Fig. 10 shows a plot of power out versus gate-2 voltage for the three frequencies measured. As shown, 18 dB of power control is achieved for the full gate-2 voltage range. Peak phase variations of 10.9°, 7.2°, and 9.5° at 9, 10, and 11 GHz, respectively, are shown in Fig. 11.

Measurements have been performed on the amplifier output network to determine the impedance presented to the output of the devices. The measured real part of circuit impedance was 18.9, 16.2, and 13.3 Ω rather than the desired 14.2, 14.6, and 13.1 at the three test frequencies. The drain bond wire inductance was not included in this measurement. However, the 9×0.7 mil bond wire was estimated to be 12 Ω of inductive reactance at 10 GHz. This mismatch at the output port is apparently responsible for the difference between the measured power of 31.3 dBm and the expected power of 31.8 dBm at 10 GHz.

VIII. Conclusions

An automated injected signal load-pull system capable of measuring active devices at power levels up to 4 W has been designed and thoroughly tested. The load-pull system was used to characterize dual-gate FET's. This technique determines the value of the drain load impedance required to yield maximum power delivered to the load while minimizing transmission phase variation. This was accomplished by measuring the S_{21} phase variation as a function of gate-2 voltage at each impedance contour. The measurement determines the intrinsic large-signal drain to source resistance for the established input RF power and dc bias conditions. Support is given to the measurement technique by the successful design and implementation of a variable power amplifier that uses devices characterized on the load-pull system.

IX. Appendix

The admittance, as seen from the left and right sides of the output reference plane (Fig. 1), is Y_L and Y_D, respectively. Assuming harmonics are short circuited, the voltage V across the plane is

$$V = \frac{(V_2^+ \times Y_O) - (V_2^- \times Y_O)}{Y_D} \tag{7}$$

and

$$V = \frac{(V_2^- \times Y_O) - (V_2^+ \times Y_O)}{Y_L} \tag{8}$$

where Y_O is the system characteristic admittance. Consequently, $Y_L = -Y_D$. Furthermore, the reflection coefficient from the left side is

$$\Gamma_L = \frac{V_2^+}{V_2^-} = \frac{Y_O - Y_L}{Y_O + Y_L} \tag{9}$$

while the reflection coefficient seen from the right side is

$$\Gamma_D = \frac{V_2^+}{V_2^+} = \frac{Y_O - Y_D}{Y_O + Y_D}. \tag{10}$$

Using $Y_L = -Y_D$,

$$\Gamma_L = \frac{Y_O + Y_D}{Y_O - Y_D} \tag{11}$$

$$\Gamma_L = \frac{1}{\Gamma_D}. \tag{12}$$

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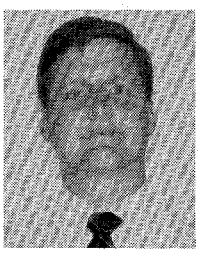
Denis M. Drury (M'79–SM'90) was born in Cape Girardeau, MO, in 1954. He received the B.S. degree in 1979 from the University of Missouri at Columbia, and the M.S. degree in 1987 from the University of Texas at Arlington, both in electrical engineering.

In 1979 he joined the Antenna Laboratory of McDonnell Douglas Corporation as a System Test Engineer. His responsibilities included the development of EMC/EMI test systems and the testing of avionics systems for the F/A-18 and F-15 aircraft. In 1984 he joined the Microwave Products and Technology Division of the Defense Systems and Electronics Group at Texas Instruments, Dallas, TX. His experience has been in the design and development of millimeter-wave/microwave modules and GaAs MMIC devices. He has been involved in phase shifter, low-noise, and power amplifier design for radar phase array and missile seeker applications.



David C. Zimmermann (M'79) was born in San Antonio, TX, in 1956. He received the B.S. and M.S. degrees in electrical engineering from the University of Texas at Austin in 1978 and 1979, respectively.

In 1979 he joined the Microwave Products and Technology Division of the Defense Systems and Electronics Group, Texas Instruments, Dallas, TX. His work at Texas Instruments has included design of diode phase shifters, switches, power amplifiers, low-noise amplifiers, and dual-gate GaAs FET devices for applications through Ku band. Currently, he leads the design and integration efforts for an X-band transmit-receive (T/R) module for phased-array radar technology.

W. Alan Davis (M'69) was born in Evanston, IL on July 1, 1941. He received the Ph.D. degree in electrical engineering from the University of Michigan in 1971.

Upon graduation he joined McMaster University, Hamilton, Ont., Canada. Subsequently he worked at the General Electric R&D Center from 1973 to 1976 where he was involved with IMPATT diode amplifiers. He then joined Raytheon where he worked on solid state transmitter and passive circuit designs. In 1983 he became Associate Professor of electrical engineering at the University of Texas at Arlington, where he is a member of the NSF Center on Advanced Electron Devices and Systems. During the 1990–1991 School year he was at Sandia National Laboratories, Albuquerque, NM, working on design of heterojunction bipolar transistors.